What is claimed:

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1. A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a bit line that is a component of the DRAM and a connection layer that is located in a common layer with the bit line and this is used to electrically connect a lower electrode of the capacitor element and another semiconductor element;

(b) simultaneously forming a storage node of the cell capacitor and the lower electrode;

(c) simultaneously forming a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

(d) simultaneously forming a cell plate of the cell capacitor and an upper electrode of the capacitor element.

2. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is carried out simultaneously with the step (d), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantation of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

3. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is carried out simultaneously with the step (d), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

4. A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(e) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (e) is carried out simultaneously with the step (d), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

5. A semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the semiconductor device comprising:

an interlayer dielectric layer, an embedded connection layer and a connection layer,

wherein the interlayer dielectric layer is located between the semiconductor substrate and the capacitor element,

the connection layer and the embedded connection layer are used to electrically connect a lower electrode of the capacitor element to another semiconductor element,

the connection layer is located in a common layer of a bit line that is a component of the DRAM,

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the embedded connection layer is located in a connection hole formed in the interlayer dielectric layer,

one end of the embedded connection layer connects to the lower electrode at a bottom surface of the lower electrode, and

another end of the embedded connection layer connects to the connection layer.

6. A semiconductor device according to claim 5, further comprising

an additional capacitor element,

wherein the additional capacitor element is located in the analog element region, and

the capacitor element and the additional capacitor element are serially connected to each other by the embedded connection layer and the connection layer.

7. A semiconductor device according to claim 5, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

an impurity concentration of the first resistance element is higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

8. A semiconductor device according to claim 6, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

an impurity concentration of the first resistance element is higher than an impurity concentration of the second resistance element so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

9. A semiconductor device according to claim 5, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

the first resistance element includes a silicide layer so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

10. A semiconductor device according to claim 6, further comprising a first resistance element and a second resistance element,

wherein the first resistance element and the second resistance element are located in the analog element region, and

the first resistance element includes a silicide layer so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

11. A semiconductor device according to claim 5, wherein a thickness of a dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of the cell capacitor.

12. A semiconductor device according to claim 6, wherein a thickness of a dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of the cell capacitor.

13. A semiconductor device according to claim 7, wherein a thickness of a dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of the cell capacitor.

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14. semiconductor device according to claim 9, wherein a thickness of a dielectric layer of the capacitor element is identical with a thickness of a dielectric layer of the cell capacitor.

10. ~~15.~~ A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a cell capacitor formed in a DRAM region of a semiconductor substrate, and a capacitor element formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a bit line that is a component of the DRAM and a connection layer that is located in a common layer with the bit line and used to electrically connect a lower electrode of the capacitor element and another semiconductor element;

forming a second conducting layer and etching a portion of the second conducting layer to form a storage node of the cell capacitor and the lower electrode;

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer of the cell capacitor and a dielectric layer of the capacitor element; and

forming a third conducting layer and etching a portion of the third conducting layer to form a cell plate of the cell capacitor and an upper electrode of the capacitor element.

11. ~~16.~~ A method according to claim ~~15~~ 10, further comprising forming a first resistance element and a second resistance element in the analog element from the third conducting layer, wherein the first resistance element and second resistance element are formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

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